

APPENDIX

Claims 1-32 (Cancelled)

Claim 33 (Previously presented): A method of manufacturing a stacked power chip resistor that increases the amount of heat dissipated without requiring additional board space comprising:

separating a first chip resistor from a second chip resistor with a glass encapsulant, each chip resistor comprising a substrate, a resistive element on the substrate and first and second end caps electrically connected to opposite ends of the resistive elements; connecting the first end cap of the first resistor and the first end cap of the second resistor with a first barrier to mechanically connect the first and second chip resistors; connecting the second end cap of the first resistor and the second end cap of the second resistor with a second barrier to mechanically connect the first and second chip resistors to provide long term mechanical stability.

Claim 34 (Previously presented): The method of claim 33 wherein each substrate is an alumina substrate.

Claim 35 (Previously presented): The method of claim 33 wherein each resistive element is a ruthenium oxide resistive element.

Claim 36 (Previously presented): The method of claim 33 wherein the first chip resistor and the second chip resistor are each of a standard size of approximately 0.250 inches in length.

Claim 37 (Previously presented): The method of claim 33 wherein the first and second metal barrier comprise nickel plating.